

REMARKS

In the present application, claims 1-14 are pending. Claims 1, 7, 9, and 11-14 are rejected by the Examiner under 35 U.S.C. §102(e). Claims 2, 3, 5, 6, and 10 are rejected by the Examiner under 35 U.S.C. §103(a). Claims 4 and 8 are rejected by the Examiner under 35 U.S.C. §103(a). In view of the foregoing, applicants respectfully request reconsideration of the application.

Rejection Under 35 U.S.C. §102(e)

In paragraph 3 of the final Office Action, claims 1, 7, 9, and 11-14 are rejected under 35 U.S.C. §102(e) as being unpatentable over Nguyen (U.S. Patent 6,308,189). Applicants respectfully traverse this rejection. Claim 1 recites in part "... a second circuit *connected* to outputs from the first circuit and configured to send at least one received signal to at least one output endpoint ..." (emphasis added).

As stated previously in the Response dated June 13, 2003, Nguyen does not teach or disclose a second circuit directly connected to outputs from the first circuit because Nguyen shows intermediary circuits such as the AND gates and the inverters in FIG. 3A. In regards to claims 1, 7, and 14, the Examiner has disagreed with this contention and recites in paragraph 7 of the final Office Action that "The AND gates and inverters are used as selection logic for the multiplexers in order for the MUX's to be properly connected to the appropriate barrel shift register." The Examiner has also asserted that the "AND gates and inverters can be considered as part of the MUX circuit since such selection logic must be present."

Both assertions that the AND gates and the inverter of Nguyen in FIG. 3 are used as selection logic and the AND gates and the inverter can be considered as part of the MUX are

incorrect. Instead, the inputs of the MUX 337-340 are selected by **the control signals 345-348**. Nguyen discloses in col. 5, lines 12-14 that “[e]ach MUXs 337-340 selects among its three input signals, each input signal including a plurality of bits, **under the control of a corresponding control signal 345-348**.” These control signals are from the dispatch unit 205 in FIG. 2 (col. 5, lines 15-16.) Further, Nguyen in col. 8, lines 20-22 recites that “[c]ontrol signals 345-348 provided to MUXs 337-340, respectively, select outputs from AND gates 335, 321, 323, and 325, respectively, for an m-bit right shift.” Clearly, the control signals 345-348 are used as selection logic for the MUXs 337-340, and the AND gates and the inverters are not used as selection logic.

Additionally, since the AND gates and the inverters are not selection logic, the AND gates and the inverters can not be considered as part of the MUX circuit. The AND gates and the inverters are used for clear masks 327-330 (col. 8, lines 11-14) and not selection logic for the MUXs. Thus, Nguyen shows intermediary circuits such as the AND gates and the inverters in FIG. 3, and Nguyen does not teach or suggest a second circuit connected to outputs from the first circuit as recited in claim 1. Therefore, claim 1 is not anticipated by Nguyen and is in condition for allowance. The same arguments for claim 1 against the Examiner assertions also apply to independent claims 7 and 14. Claim 9 and 11 depend directly from claim 7 and are therefore allowable for at least the same reasons as claim 7. Claims 12 and 13 depend directly from claim 1 and are therefore allowable for at least the same reasons as claim 1.

Rejections Under 35 U.S.C. §103(a)

In paragraph 5 of the final Office Action, claims 2, 3, 5, 6, and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nguyen (U.S. Patent 6,308,189). Claims 2, 3, 5, and 6

depend either directly or indirectly from claim 1 and are therefore allowable for at least the same reasons.

In regards to claim 2, Nguyen has already been shown to be an ineffectual reference, as it does not anticipate claim 1. Additionally, one skilled in the art would not have used the apparatus taught in Nguyen to receive the input signal including a plurality of data channels. The apparatus in Nguyen is for logical word shifts where the input signal includes operands for instructions. (col. 5, lines 56-57 and col. 5, line 65 – col. 6, line 1). Having data channels interleaved into the operands for instructions simply is illogical because the operands would have corrupt data for logical operations. Therefore, one skilled in the art would not use the apparatus in Nguyen with input signals including a plurality of channels interleaved therein, and claim 2 is allowable.

In regards to claim 3, Nguyen has already been shown to be an ineffectual reference, as it does not anticipate claim 1 and 2. Additionally, as discussed above, the multiplexer in Nguyen is not directly connected to the barrel shift register because of the intermediary circuits such as the AND gates and the inverters. Therefore, claim 3 is allowable.

Claim 10 depends from claim 7 and is therefore allowable for at least the same reasons.

In paragraph 6 of the final Office Action dated August 18, 2003, claims 4 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nguyen (U.S. Patent 6,308,189) in view of Phelps (U.S. Patent 4,512,018). Applicants traverse. Claim 4 depends directly from claim 1 and is therefore allowable for at least the same reasons. Claim 8 depends directly from claim 7 and is therefore allowable for at least the same reasons.

CONCLUSION

In view of the above remarks, Applicants believe that the rejections in the final Office Action are fully overcome, and the application is in condition for allowance. The Examiner is invited to call Applicants' representative at the number below if he has any questions or if there are remaining outstanding issues.

Respectfully submitted,

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